New Tools and Standards Boost Embedded Systems Performance

Embedded Tech Trends
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Pentek, Inc.
Topics

- New Challenges for Real-time Embedded Systems
- Evolving Xilinx FPGA Technology
- JESD204B Gigabit Serial Peripheral Interfaces
- AXI4 Interconnect Standard
- Navigator Design Tools
Challenges for Real-Time Embedded Systems

- Increased Component Density
- Higher Device Complexity
- Higher-Speed Data Converters
- Faster Device and Board Interfaces
- Longer Development Cycles
- New Technology Insertion
- Design Portability
- Reliability and Maintainability
- Life Cycle Management
- SWaP-C

- New Device Technology
  - Geometry and process improvements
- Faster Interconnect Technology
  - Migration to gigabit serial links
- Open Hardware Standards
  - Boards, Backplanes, & Chassis
  - Links, Protocols & Interfaces
- Open FPGA Standards
  - HDL & Module Interfaces
- Graphically Oriented Design Tools
  - Block Diagram Design Entry
- High-Level Software Tools
  - API with Layered Modules
Evolution of Xilinx FPGA Series

FPGAs available in 35x35mm and 42.5x42.5mm BGA packages
### Comparing Virtex-6, Virtex-7, & Kintex UltraScale

<table>
<thead>
<tr>
<th>Category</th>
<th>Virtex-6</th>
<th>Virtex-7</th>
<th>Kintex UltraScale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>476k</td>
<td>693k</td>
<td>1451k</td>
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<tr>
<td>Maximum DSP48E1 Slices</td>
<td>2016</td>
<td>3600</td>
<td>5520</td>
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<td>SDRAM Memory Speed</td>
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<td>DDR4 2400 MHz</td>
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<td>Maximum Block RAM</td>
<td>38 Mbits</td>
<td>53 Mbits</td>
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<td>Max Configurable Logic Blocks</td>
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<td>305k</td>
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<tr>
<td>Relative I/O Power</td>
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<td></td>
<td>100%</td>
</tr>
<tr>
<td>Relative Dynamic Power</td>
<td></td>
<td></td>
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<tr>
<td>Relative Maximum Static Power</td>
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<td>100%</td>
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### Virtex-6, Virtex-7 & Kintex UltraScale Comparisons

<table>
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<tr>
<td>LX130</td>
<td>128K</td>
<td>326K</td>
<td>444K</td>
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<td>LX240</td>
<td>241K</td>
<td>693K</td>
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<tr>
<td>SX315</td>
<td>314K</td>
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<table>
<thead>
<tr>
<th>DSP slices</th>
<th>Virtex-6</th>
<th>Virtex-7</th>
<th>Kintex UltraScale</th>
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<td>480</td>
<td>1120</td>
<td>1700</td>
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<td>768</td>
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<td>1344</td>
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</tbody>
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- **Excellent range of FPGA resources for the same XMC I/O function**
  - Scalable by more than a factor of 10
  - Customer can choose the most cost effective solution
  - Eases upgrades and new technology insertion
  - Minimizes life cycle support issues

- **Kintex UltraScale Compared with Virtex-6 and Virtex-7**
  - Cost per Logic Cell and DSP Slice Reduced by 30% to 50%
  - Power dissipation reduced by 20% to 40%
Factory Installed FPGA Features Simplify Development

- Acquisition Engines
  - Pre-Triggering & Delayed-Triggering
  - Radar Range Gate Generation
  - Synchronous across boards
- Multiband Digital Downconverters
  - Decimation from 2 to 65K
  - Bandwidths from 80 MHz to 3 kHz
- Real Time Power Meters
  - Energy detection
  - Programmable threshold interrupts
- Metadata Generators
  - Precise Time-stamping
  - Channel ID & block counter
- Linked List DMA Controllers
  - Delivers Data Blocks across PCIe to System Memory
Traditional Data Converters Use Parallel LVDS I/O

- Each clock or clock edge transfers one bit for each data sample
- Data clock and A/D clock are the same – one sample per clock
- Example: A 12-bit A/D requires one LVDS pair per bit

Advantages

- Simple
- Easy to change sample rate with no changes in the FPGA

Disadvantages

- Consumes FPGA I/O pins
- Requires many PCB traces - eats up real estate & layers
- High speed data converters need multiple banks of LVDS pairs

LVDS

12 LVDS Pairs
= 24 PCB traces

Texas Inst ADS12D1800
3.6 GHz
12-bit A/D

FPGA

Aggregate Rate: 5.4 GB/sec
JEDS204B Gigabit Serial Data Converter Interfaces

- **JESD204B Gigabit Serial Interface**
  - Gigabit serial links up to 12.5 Gbaud
  - Different data framing for each mode
  - Data scrambler, alignment codes, 8B10B channel coding, idle patterns, etc.

- **Advantages**
  - Far fewer traces, but require strict layout and matching
  - Uses native GTX and GTH gigabit serial I/O pins of FPGAs
  - Supports higher sample rates, DDCs, and channel counts

- **Disadvantages**
  - Many data frame modes including DDC modes with different bandwidths
  - Converter sample rate and gigabit serial rates are locked at fixed ratio
  - Changing sample rates and modes requires changing JESD204B clock rate of the FPFA JESD204B receivers – inconvenient!

- **COTS vendors must abstract these complexities from the user**
  - Requires extensive investments in software and FPGA tools
AXI-4 Standard – What Is It?

- AXI (Advanced eXtensible Interface) is part of the ARM® AMBA® (Advanced Microcontroller Bus Architecture)
- It is an open standard, on-chip interconnect specification for functional blocks in SoC (system-on-chip) designs
- The AMBA 4 AXI4 specifications were introduced in 2010
- Due to larger and more complex IP for FPGAs, Xilinx adopted AXI4 as the interface standard for IP blocks to communicate in their Vivado tools
- Now both Xilinx and Altera have embraced AXI4 not only for interconnecting FPGA IP blocks, but also for on-chip processors and peripherals
Why Use AXI4 in FPGAs?

- AXI4 handles much of the “housekeeping” like matching speeds and data widths between blocks.
- Customers who follow the AXI4 guidelines when creating custom IP from scratch can expect the IP to connect to existing AXI4 IP.
- AXI4 eases integration and interfacing of IP cores from vendors like Xilinx and other third parties with “plug and play” compatibility.
- AXI4 abstraction of interconnects simplifies graphically oriented block diagram-type design environments such as the Xilinx IP Integrator.
- Entire buses can be abstracted into single “wires.”
- Improves productivity, portability and reusability.
Pentek Navigator IP is delivered as AXI4 Blocks
Designing IP with VHDL
Graphical AXI4 IP Design with Xilinx Vivado IP Integrator

Pentek AXI4 IP

Xilinx AXI4 IP
- Direct mapping of BSP API Functions and FPGA IP Modules simplifies software support for customer developed IP.
52131: 8-Ch 250 MHz 16-bit A/D + DDCs 3U VPX Module

- Kintex UltraScale FPGA
  - KU035, KU060, or KU115
- Eight 250 MHz 16-bit A/Ds
  - Texas Inst ADS42LB69
  - Full 200 MHz Bandwidth
  - JESD204B Interfaces
- Eight Multiband DDCs
  - Decimation from 2 to 64K
- 5 GB DDR4 2400 MHz SDRAM
- VITA 66.4 Optical I/O
  - 8 GB/sec to Backplane
- PCIe Gen 3 x8
- Sample Clock Synthesizer
- Multi-channel Synchronization
- Navigator FPGA Design Kit
- Navigator Board Support API
- Releasing at ETT Show Today!
Solutions for Real-Time Embedded Systems

- **New Device Technology**
  - Geometry and process improvements

- **Faster Interconnect Technology**
  - Migration to gigabit serial links

- **Open Hardware Standards**
  - Boards, Backplanes, & Chassis
  - Links, Protocols & Interfaces

- **Open FPGA Standards**
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- **Graphically Oriented Design Tools**
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- **High-Level Software Tools**
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- **Kintex UltraScale FPGA**
  - More Resources, Lower Power & Cost

- **JESD204B Interconnect Standard**
  - Faster, fewer wires, less space

- **VITA 66.4 Optical Backplane**
  - Blind mating, eliminates front connectors
  - Fast, long distance data links

- **AXI4 IP Interconnects**
  - Graphical design, portability, reusability

- **Xilinx Vivado IP Integrator**
  - Graphically connects AXI4 IP Blocks

- **Pentek Navigator Tool Suite**
  - API Libraries, AXI4 FPGA IP Blocks
Thank You!! — Questions??