Addressing the Platform Challenges of Next Generation Electronic Warfare Systems

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Electronic Warfare

Electronic Attack

Electronic Protect

Electronic Warfare Support
Typical Electronic Attack Mission
Traditional Electronic Warfare System

- **SBC347D**
  - Intel Xeon D
  - 32 GB DDR4

- **FMC170**
  - 5GSPS
  - Low Latency ADC

- **VP780**
  - FPGA w/FMC

- **FMC170**
  - 5GSPS
  - Low Latency DAC

- **GRA113**
  - NVIDIA GM107
  - 640-core GPU
EW Platform Challenge: Latency

End to End Latency Must be Minimized

- SBC
- FPGA
- GPU
- RF
- ADC
- DAC
- Memory
- VITA 57.1
- VITA 57.4
- JESD204B
- LVDS
- FMC170 5GSPS Low Latency ADC
- FMC170 5GSPS Low Latency DAC
VITA 57.1 & VITA 57.4 Pinout

Favors High Speed Serial Bus Going Forward

High Speed Serial Lane (Higher Latency, Higher Data Rates)

Parallel Data Bus (Lower Latency, Parallel Buses Required)

JESD204B (5 Lanes)

[Clocks]

[Sync]

[Power]

LVDS (22 Pairs)

JESD204B (1 Lane)

LVDS (12 Pairs)

JESD204B (9 Lanes)

LVDS (9 Lanes)

LVDS (22 Pairs)

LVDS (24 Pairs)

JTAG & Power

VIO

VADJ

VADJ

Parallel Data Bus

FM C+

FM C

LPC Connector

LPC Connector

HPC Connector

HSPC Connector

Abaco Systems
EW Platform Challenge: Resources & IP Security
EW Platform Challenge: ‘Use the Right Tool’

- **SBC**
  - Ideal for Cognitive EW, Complex Branching Execution
  - SBC347D Intel Xeon D 32 GB DDR4

- **GPU**
  - Ideal for deep learning neural net processing
  - GRA113 NVIDIA GM107 640-core GPU

- **FPGA**

- **DAC**

- **RF**

- **ADC**

- **Memory**

Highspeed data bus
Challenges of Next Generation EW Systems

- Large FPGA Fabric
- Required I/O Count
- IP Security
- Anti-Tamper
- Latency Optimized
- Synchronous
- Multi-Channel
- Wide Bandwidth
- GPUDirect RDMA
- C/C++ Languages
- High Performance DSP Functions
- High Performance
- Data Connection
- VITA 65
- Open VPX
- Fiber Connect
- Noise Performance
- SNR
- Dynamic Range
- Spectral Purity and Distortion
- High Power Output
- (GaS / GaN)

- Reduced Size
- Reduced Weight
- Reduced Power
- Reduced Cost
- Processor Architecture
- Cognitive EW Algorithms
- C/C++ Languages
- Latency Optimized
- Synchronous
- Multi-Channel
- Wide Bandwidth
- Large FPGA Fabric
- Required I/O Count
- IP Security
- Anti-Tamper
- Latency Optimized
- Synchronous
- Multi-Channel
- Wide Bandwidth
- GPUDirect RDMA
- C/C++ Languages
- High Performance DSP Functions

3U VPX

RF → ADC → FPGA → DAC → RF

highspeed data bus

SBC

GPU

Memory

abaco SYSTEMS
VPX167 COTS Airborne Pod Platform

FlexVPX Backplane 7 Slots

SBC347D
Intel Xeon D
32 GB DDR4

FMC170
5GSPS
Low Latency ADC

VP780
FPGA w/FMC

FMC170
5GSPS
Low Latency DAC

GRA113
NVIDIA GM107
640-core GPU

Power Supply

Local Oscillator

10MHz Reference

Power Supply
WE INNOVATE. WE DELIVER. YOU SUCCEED.