HOST - A Key Pillar of NAVAIR R’s Open Architecture Approach
Key Goals

“Provides a framework for developing embedded computing systems for U.S. military platforms. HOST provides U.S. Government Acquisition, System Integrators, and Third Party HOST Component Vendors with an open, interoperable, upgradeable, and sustainable embedded system standard.”
HOST Benefits

Old Paradigm

Circuit Card Assembly

Custom Functionality Defined by Integrator

Custom Set of Cards

Inter Card Jumpers Complicates Wiring

New Paradigm

HOST Assembly

Standardized Interfaces to Provide Functionality

Standardized Set of Cards

Utilizes Defined Interfaces Over Back, and Mid Plane

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The HOST Standards

TIER I: CORE TENETS (Single Document)
Preserve HOST “openness” by establishing universal requirements that apply to all HOST components regardless of core technology

TIER II: CORE TECHNOLOGIES (Document for each core technology chosen)
Define platform agnostic technical requirements for core technologies (Examples are OpenVPX, PC104, and VME)

TIER III: COMPONENT SPECIFICATIONS (Many Documents)
These are component level documents that will guide H/W development to facilitate modular components, Tier III reuse, and upgradeability

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Tier 1 HOST Components

- HOST Components
  - Enclosures, Transmission Components, External Interfaces and Modules

Figure 4-2 – Example HOST Component Categories
Tier 1 HOST-Management (HOST-MGMT)

Autonomous subsystem that provides application independent hardware management and monitoring capabilities

Logical control elements for HOST-MGMT representation
Managers (chassis-level) and Participants (module-level)

Manager/Participants Protocol (MPP) defines standardized means of data exchange
## Tier 2 Payload Modules

<table>
<thead>
<tr>
<th>Profile Name</th>
<th>Data Plane 4 FP</th>
<th>Expansion Plane 4FP</th>
<th>Control Plane 2 UTPs</th>
<th>Control Plane 2 TPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOD6-PAY-4F1Q2U2T-HOST</td>
<td>DP01 – DP04</td>
<td>DP01 – DP04</td>
<td>CPutp01</td>
<td>CPtp01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CPutp02</td>
<td>CPtp02</td>
</tr>
</tbody>
</table>

### Key
- User Defined
- Control Plane – 2 Ultra-Thin Pipes
- Control Plane – 2 Thin Pipes
- Data Plane – 4 Fat Pipes
- User Defined
- Expansion Plane – 4 Fat Pipes

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**T2-PER-0045**: Payload Modules may implement 10GBASE-KR on the Control Plane UTPs.

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Tier 2 Switch Modules

Profile 1

Profile 2
Tier 2 Payload Modules

Figure 5-2 – HOST Payload Slot Profile, SLT3-PAY-2F2U-HOST

<table>
<thead>
<tr>
<th>Profile Name</th>
<th>Data Plane 2 FP</th>
<th>Control Plane 2 UTPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOD3-2F2U-HOST</td>
<td>PCIe per ANSI/VITA 65-2010 Section 5.3</td>
<td>1000BASE-KX or BX per ANSI/VITA 46.6</td>
</tr>
</tbody>
</table>

T2-PER-0045: Payload Modules may implement 10GBASE-KR on the Control Plane UTPs.
Tier 2 Switch Modules

Profile 1

Profile 2

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Tier 2 Payload Modules

- **Mezzanine Mapping**
  - HOST calls out specific ANSI/VITA 46.9 I/O mapping for Payload Modules that have Mezzanine sites.
  - 46.9 calls out ways for Plug-In Modules to route I/O from their Mezzanine Sites to the backplane connector (i.e., RT 2-R) wafers.

From VITA46.9

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