New Initiatives and Technologies
Brighten Embedded Software Radio

Embedded Tech Trends
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Sensor Open System Architecture (SOSA)

- Consortium of Air Force, Navy, Army, DoD, Industry, & other Government Agencies
- Develop & Adopt Open Systems Architecture standards for C4ISR
- Common multi-purpose backbone architecture for Radar, EO/IR, SIGINT, EW, & communications
- Platform affordability, rapid fielding, re-configurability & overall performance
- Re-purposing of hardware/software/firmware
- Business/acquisition practices to foster innovation, industry engagement and competition
Modular Open RF Architecture - MORA

- CERDEC’s evolving definition of converged open architecture for open interfaces to enable rapid insertion of new capabilities, interoperability, and a reduced SWaP footprint
- MORA extends the U.S. Army’s VICTORY architecture for vehicle electronics
- Share hardware and software components among C4ISR/EW capabilities
- Allow technology refresh to keep pace with threats while improving reliability & robustness
- Support interoperability requirements and facilitate transition planning
- Permit innovative unplanned capabilities for quick-reaction “future-proofing”
- Reduce developmental and acquisition costs through greater commercial competition
VITA 49 – Virtual Digital RF Transport Protocol (VRT)

- Traditional radios used stovepipe architectures
  - Application specific, custom analog RF and IF signal cabling & switching
  - Proprietary digital links and switches
  - Each system was dedicated to a specific radio application

- VITA 49 – VRT
  - Flexible RF transceivers deliver and accept digitized signals using a standardized packet protocol
  - Switching, routing and distribution is done across a COTS digital network
  - Metadata, control, and status packets are linked to the digital signal packets
  - Configurable for a wide range of applications using the same hardware
Initial Evolution from VICTORY to MORA

- VICTORY Shared Processing Unit
- Gigabit Ethernet Switch
- VITA 49 Radio Data
- MORA High-Speed Bus - 10 GbE
- VICTORY Data Bus - GbE
- RF Cables
- Power Bus
- Software Defined Radio Boards
- RF Distribution Unit
- Radio Heads Antennas
- RF / IF Power Amps
Later Evolution from VICTORY to MORA

- VICTORY Shared Processing Unit
- Gigabit Ethernet Switch
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- Power Bus
- Software Defined Radio Boards
- RF Distribution Unit
- Radio Heads
  - Antennas
  - RF / IF Power Amps
  - Data Acquisition Modules
  - A/Ds + D/As
MORA Component Requirements for Board Vendors

- OpenVPX Architecture compliant with applicable VITA standards
- Interchangeable system components for reconfiguration and new technology insertion
- 10 GbE interfaces for digitized C4ISR data signals (evolving to 40 & 100 GbE)
- 1 GbE interfaces for control and status
- VITA 49 protocol engines for C4ISR data
- Runtime reconfigurable via processor software and FPGA IP
- Scalable channel count, bandwidth, and processing power
- Synchronous acquisition across multiple RF channels and multiple chassis
- Backplane I/O when possible for copper and optical digital, timing, and RF signals
New Technologies and Standards Serve the Mission

- **Kintex UltraScale FPGAs**
  - 5520 DSP Engines
  - Over a million logic cells
  - Lower power and cost

- **Fast A/D and D/A Converters**
  - Sample Rates to 6.4 GS/sec
  - High density – low power

- **JESD204B Device Interfaces**
  - Reduces number of PCB traces by 12 times
  - Supports ADCs & DACs to 6 GS/sec and higher

- **VITA 57.4 FMC+**
  - HSPC connector with 80 LVDS + 24 serial lanes
  - HSPCe connector adds 8 more serial lanes
  - Gigabit serial rates to 28 Gbaud

- **VITA 49.2 Radio Transport**
  - ANSI/VITA Approved in 2017
  - Receive & Transmit Protocols
  - Control & Status Protocols
  - Precision Timing Protocols
  - Comprehensive Infrastructure
New Technologies and Standards Serve the Mission

- **VITA 66.x Optical Backplane VPX I/O**
  - Several full- and half-width blind-mate optical connector types
  - Provides high bandwidth data paths between boards and chassis

- **VITA 67.x Coax Backplane VPX I/O**
  - Several multi-position connector types – up to 12 coax signals
  - RF signal bandwidths to 40 GHz
  - Eliminates front panel signal cables

- **VITA 65.0 & VITA 65.1 OpenVPX - 2017**
  - Major enhancements reflect widespread use and adoption of OpenVPX
  - New Card, Slot and Backplane Profiles
  - Radial Backplane Clock distribution ensures precision timing and synchronization across boards
  - Provision for a 100 MHz reference clock
  - New definitions of combinations of VITA 66.x optical and VITA 67.x coaxial backplane I/O
Inherits Jade XMC Architecture
- Navigator BSP and FDK Tools

Powerful Kintex UltraScale FPGA
- KU060, KU085, or KU115

x8 PCIe Gen 3 for 8 GB/sec peak rate

4x Gigabit Serial User I/O

16-pairs LVDS User I/O

Optional Precision GPS Receiver
- 10 MHz Freq ReF + 1 PPS for Time Stamp
- Flywheel mode with OCXO accuracy

9 GB DDR4 SDRAM
- 2400 MHz Data Transfer Rate

Optional VITA 66.4 Optical Backplane
- 12 GB/sec full duplex data transfers

FMC or FMC+ Site
- VITA 57.1 HPC: 160 LVDS + 8x GTH
- VITA 57.4 HSPC: 160 LVDS + 24x GTH

VITA 49.2 Protocol Engine
2-Channel Wideband Analog I/O FMC Module

- Two 3.0 GHz 14-bit A/Ds
  - Texas Inst ADC32RF45
  - 3 dB input BW: 3.2 GHz
  - Two Digital Downconverters
- Two 2.8 GHz 16-bit D/A s
  - Texas Inst DAC39J84
  - Two Digital Upconverters
- Timing Bus Generator
  - Programmable Clock Synthesizer phase-locked to 10 MHz input reference
  - Synchronization across multiple boards
  - Full triggering, gating and time-stamping
- 2-Channel wideband transceiver or transponder for communication and radar
Addressing MORA Requirements Today

OpenVPX 3U Chassis

- Single Board Computer
  - Intel CPU
  - Linux or Windows
- FMC Connector
  - A/D
  - D/A
  - Clock
- Kintex Ultra Scale FPGA with VITA 49
- JadeFX Model 5983
  - PCIe Gen 3 x8
  - 10/40 GbE
  - Optical I/F
- SSD
- SDRAM
- BIOS FLASH

Power Bus

VICTORY Data Bus

MORA High-Speed Bus

RF Cables

Software-Defined Radio

Radioheads (Antenna + PA)

RF Distribution Device

VICTORY Shared Processing Unit

PCIe x4

1 GbE

RS232

USB

PCIe

Power Bus

Power Bus

Power Bus

Power Bus

Power Bus
- Performs analog/digital conversion for transmit and receive signals
- Includes digital up and down conversion, synchronization, and time stamping
- VITA 49.2 engine
- But, ……requires two boards
UltraScale + SoM 3U VPX JadeFX FMC Carrier

- Adds System-on-Module (SoM) to Model 5983
- SoM ARM Cortex-A9 System Controller
  - Linux OS
  - 1 GbE Port for Control and Status
  - 1x PCIe Link to Kintex UltraScale
  - Dedicated 1 GB DDR3 SDRAM
  - Non-volatile SD Memory Card
  - USB Ports for peripherals
- SoM Functions/Benefits
  - Replaces SBC for many applications
  - Complete Sub-system
  - Reconfigures the FPGA over GbE
  - Control and Monitoring over GbE
MORA Remote Data Acquisition Modules – Take 2

- Complete stand-alone, single board solution for MORA data acquisition
- Local ARM processor implements API for simplified programming and control
- FPGA is reconfigurable via 1 GbE
- Interchangeable front ends for flexibility in channel count and signal bandwidth
- Range of FPGA devices to match horsepower requirements
- GbE and 10 GbE network switches allow virtually any number of nodes
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Thank You!! – Questions??

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